12-GHz-Band GaAs Dual-Gate MESFET Monolithic Mixers

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Abstract—12-GHz-band GaAs dual-gate MESFET monolithic mixers have been developed for use in direct broadcasting satellite receivers. In order to reduce chip size, a buffer amplifier has been connected directly after a mixer IF port, instead of employing an IF matching circuit. The mixer and the buffer were fabricated on separate chips, so that individual measurements could be achieved. Chip size is 0.96×1.26 mm for the mixer and 0.96×0.60 mm for the buffer. A dual-gate FET for the mixer, as well as a single-gate FET for the buffer, has a closely spaced electrode structure. Gate length and width are 1 μm and 320 μm, respectively. The mixer with the buffer provides 2.9±0.4-dB conversion gain with 12.3±0.3-dB SSB noise figure in the 11.7–12.2-GHz RF band. Local oscillator (LO) frequency is 10.8 GHz. A low-noise converter was constructed by connecting a monolithic pre-amplifier, an image rejection filter, and a monolithic IF amplifier to the mixer. The converter provides 46.8±1.5-dB conversion gain with 2.8±0.2-dB SSB noise figure in the same frequency band.

I. INTRODUCTION

RECENT ADVANCES in GaAs technology have made monolithic microwave integrated circuits (MMIC's) more practical. Promising applications for this technology include inexpensive receiver front-ends for direct broadcasting satellite (DBS) systems [1]–[4]. 12-GHz-band low-noise GaAs monolithic amplifiers for use in DBS receivers have already been developed and reported [4]. This paper describes design considerations and performances for newly developed 12-GHz-band GaAs dual-gate MESFET monolithic mixers. Performances for a low-noise converter, which was constructed by connecting the monolithic pre-amplifier, an image rejection filter, and a monolithic IF amplifier to the mixer, are also described.

For MMIC's used in DBS receivers, a simple and highly reproducible fabrication process and small chip size are required for meeting low-cost objectives. For the first requirement, an IC process using ion-implanted closely spaced electrode FET's, which was successfully employed in fabricating monolithic amplifiers [4], [5], can be applied to the mixers' fabrication. For the second requirement, it is necessary to reduce the size for filtering and IF matching circuits because these circuits require the most area on a chip.

To reduce the filtering circuits' size, a dual-gate MESFET has been employed as a mixing device. Because the dual-gate FET has a built-in isolation effect among its electrodes, the filtering circuits can be greatly simplified [1]. In a mixer for the DBS receivers, a multisection matching circuit is necessary for an IF port, because a large bandwidth ratio is usually required for the IF band. Therefore, the IF matching circuit requires the most area on a chip, other than the filtering circuit. In this work, chip size reduction is accomplished by introducing a buffer amplifier following directly after the mixer IF port, instead of employing the IF matching circuit. In addition to the chip size reduction, this approach is suitable for MMIC's because IF port characteristics become less sensitive to variation in element parameters, compared with using the matching circuit.

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II. CIRCUIT DESIGN

A. Mixer and Buffer Amplifier

Fig. 1 shows an equivalent circuit for the mixer with the buffer. The designed RF band is 11.7–12.2 GHz, which is the DBS system frequency band. The local oscillator (LO) frequency is 10.8 GHz. Therefore, the IF band is 0.9 to 1.4 GHz. The RF and LO powers are injected into the first and the second gates, respectively, and the IF power is extracted from the drain. The impedance conditions at each port of the FET for optimum conversion gain are power matched for the corresponding frequency component and short circuit for other frequency components [6], [7]. In practical monolithic technology, however, these conditions are difficult to fulfill simultaneously. Therefore, only three conditions, power matched at the RF and LO ports and short circuit for LO frequency at the IF port, have been considered in the design. The RF and LO ports matching is realized by one-section parallel and series microstrip lines. For the LO port, the lines are shortened with a parallel capacitor. A quarter wavelength microstrip spiral stub is employed at the drain to realize an LO short circuit. Gate length and width for the dual-gate FET are 1 μm and 320 μm, respectively.

The buffer amplifier is a one-stage resistor–capacitor coupled amplifier. Input resistance for the buffer, or load resistance for the mixer, is determined by a resistor shown as R_l in Fig. 1. Drain bias voltage for the mixer FET is fed through the resistor. The single-gate FET for the buffer has 1-μm gate length and 320-μm gate width. These values are the same as for the mixer dual-gate FET.

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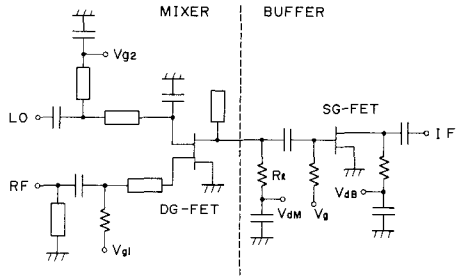


Fig. 1. Equivalent circuit for mixer with buffer.

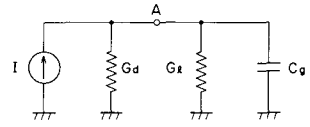


Fig. 2. Equivalent circuit for mixer–buffer interstage.

B. Mixer–Buffer Interstage

An IF band equivalent circuit for the mixer–buffer interstage is shown in Fig. 2, where I represents an equivalent current source for the mixer IF output signal, G_d is the drain conductance for the mixer FET, G_l is the conductance for the resistor R_l, and C_g is the gate capacitance for the buffer FET.

Input voltage V for the buffer, voltage V across conductance G_l, is derived as

$$V = I(G_d + G_l + j\omega C_g). \tag{1}$$

The design objective is to increase V without a large frequency dependence. For this purpose, C_g must be small, or a narrow-gate FET is preferable for the buffer. However, gain and noise-figure values for the buffer improve when a wider gate FET is used. To compromise between these requirements, the gate width was chosen at 320 μm, where C_g is 0.5 pF. The load resistance was designed at 250 Ω ($G_l = 4$ mS), taking $G_d = 2$ mS into consideration.

Fig. 3 shows three kinds of interstage circuit. Circuit (a) is the proposed circuit. Circuit (b) uses a matching network, while retaining the 250-Ω load resistance. Circuit (c) is a conventional circuit, where mixer output is matched to 50 Ω and input impedance for the IF amplifier is maintained at 50 Ω by the parallel resistor. Conversion gain and noise figure for these circuits are discussed.

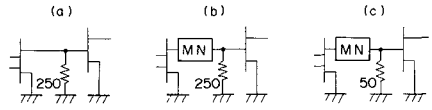
When matching is performed, voltage V_m across the load conductance G becomes

$$V_m = I\sqrt{G/G_d}/(2G + j\omega C_g). \tag{2}$$

Therefore, power loss L due to imperfect matching is given by

$$L = |V_m/V|^2 = G\left[(G_d + G_l)^2 + (\omega C_g)^2\right]/G_d\left[(2G)^2 + (\omega C_g)^2\right]. \tag{3}$$

For circuit (b), $G = 4$ mS, L at the center IF of 1.15 GHz is 1.3 (1.1 dB). For circuit (c), $G = 20$ mS, L becomes 0.30 (−5.2 dB), which means that matching to 50 Ω is worse than direct connecting to the buffer with higher input



	(a)	(b)	(c)
GAIN (dB)	2 9	4 0	−2 3
NF (dB)	1 2 3	1 1 9	1 3 1

Fig. 3. Three kinds of interstage circuit and predicted performances.

resistance. In Fig. 3, the 2.9-dB gain for circuit (a) is an experimental result.

The noise figure for the mixer is independent from the IF port matching, because an output circuit does not affect the noise figure. Thus, the noise figure for the buffer amplifier will be considered. Noise figure F_l for the input conductance G_l is given by

$$F_l = (G_d + G_l)G_d \tag{4}$$

which is a reciprocal of available gain. Noise figure F_f for the FET is given as follows, under the low-frequency approximation [8]:

$$F_f = F_0 + R_n(G_d + G_l) \tag{5}$$

where F_0 is the minimum noise figure and R_n is the noise resistance for the FET. Because G_l and FET are cascaded, the composite noise figure F can be derived by using the Friis formula [9] as follows:

$$F = F_l \times F_f = (G_d + G_l)\left[F_0 + R_n(G_d + G_l)\right]/G_d. \tag{6}$$

Substituting measured values $F_0 = 1.1$ (0.4 dB) and $R_n = 60$ Ω into (6), F can be calculated. For circuit (a), $G_d = 2$ mS and $G_l = 4$ mS, F is calculated as 4.4 (6.4 dB). When the IF output port is matched to a conductance G, G_d becomes G in (6). Thus, for circuit (b), $G_d = G_l = 4$ mS, F becomes 3.2 (5.0 dB). For circuit (c), $G_d = G_l = 20$ mS, F becomes 7.0 (8.5 dB). Therefore, the noise figure for the IF amplifier is also degraded by matching the latter to 50 Ω. In Fig. 3, the calculated total noise figures are tabulated using the measured mixer noise figure of 11.1 dB and the available gain of −0.9 dB.

From these results, it is concluded that matching to 50 Ω has no merit, as long as a resistor–capacitor coupled-type IF amplifier is employed, and that the input resistance for the amplifier should be chosen to be as large as possible within the limitation for maintaining gain flatness. When keeping the resistance high, mixer performances are somewhat improved by IF port matching. The improvement, however, is a minor problem, as compared with chip size expansion, from a practical point of view, because, as a DBS receiver, a low-noise pre-amplifier is employed in front of the mixer.

III. Fabrication Process

The mixer and the buffer were fabricated on separate chips so that individual measurements could be achieved. Figs. 4 and 5 show chip photographs for the mixer and the

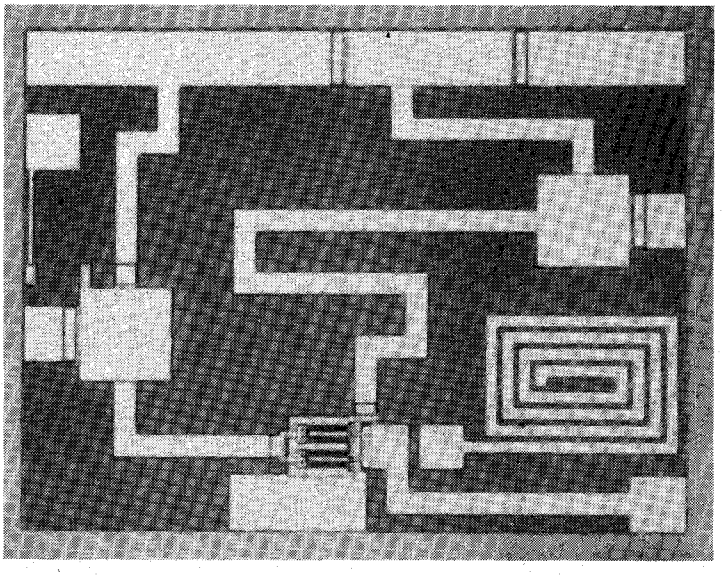


Fig. 4. Mixer chip photograph.

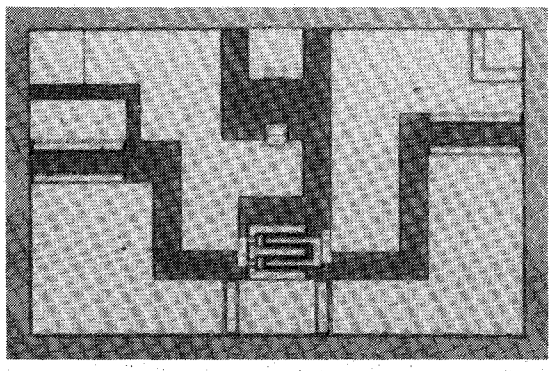


Fig. 5. Buffer chip photograph.

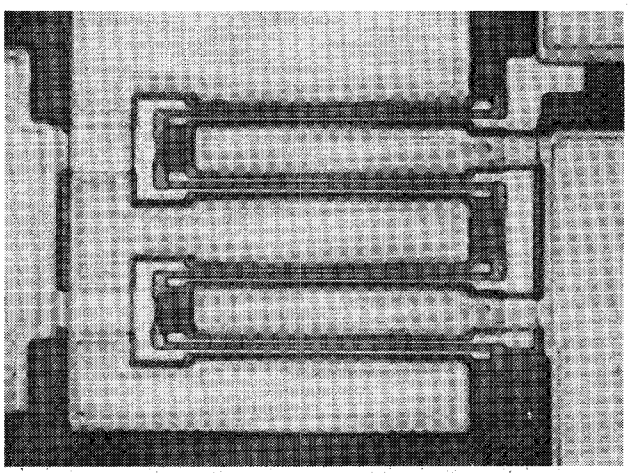


Fig. 6. Dual-gate FET electrode pattern.

buffer, respectively. Chip size is 0.96×1.26 mm for the mixer and 0.96×0.60 mm for the buffer. Both chips are 150 μm thick. A Cr-doped semi-insulating HB-grown GaAs wafer is used as the substrate. The doped Cr concentration is 0.5 wt/ppm, which corresponds to 3×10^{16} cm^{-3}.

The dual-gate FET for the mixer, as well as the single-gate FET for the buffer, have closely spaced electrode structures [4], [5]. The electrodes have an interdigital pattern with 80-μm-long Al gate fingers. Gate length and width are 1 μm and 320 μm, respectively. Ohmic electrodes are made of AuGe-Ni. The FET is passivated by an SiO_2 film. Fig. 6 shows the dual-gate FET electrode pattern.

The FET active layers were formed by selective $^{30}Si^+$ ion implantation. Implanting conditions are 70-keV acceleration energy and 3.3×10^{12} cm^{-2} dose. Then, annealing for activation was accomplished with an SiO_2 cap at 800°C for 20 min in an H_2 ambient. Fig. 7 shows static characteristics for the dual-gate FET, supplying a bias voltage at the first gate and leaving the second gate open. Threshold voltage V_t is -1.0 V and transconductance g_m at saturated drain current I_{dss} is 37 mS (116 mS per mm gate width).

The resistive layers were also formed by ion implantation. Implanting conditions are 130-keV energy and 3.8×10^{12} cm^{-2} dose, which provide 1-kΩ sheet resistance for a square resistor. The capacitors are of the MIM type, where the dielectric material is 300-nm-thick CVD-SiO_2, whose relative dielectric coefficient ϵ_r is 4.8. The microstrip lines were formed by Ti-Pt-Au lifting-off and thickened to 2.5 μm by Au plating.

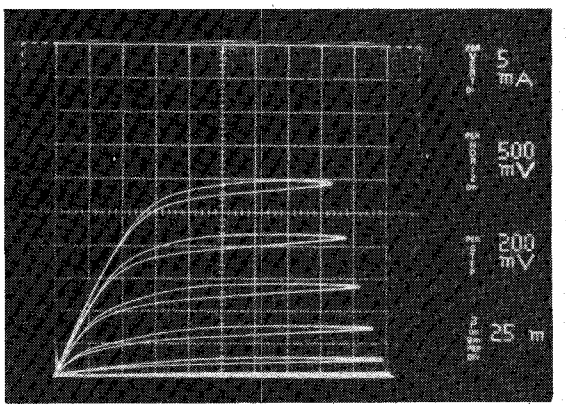


Fig. 7. Dual-gate FET static characteristics.

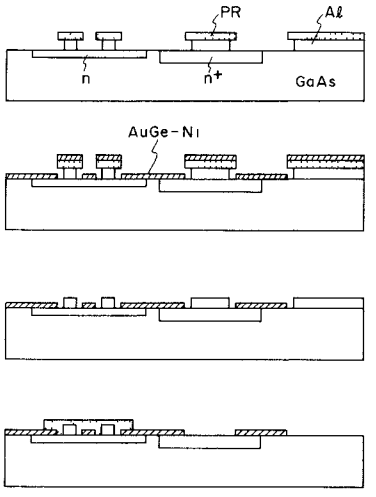


Fig. 8. Key process for closely spaced electrode FET.

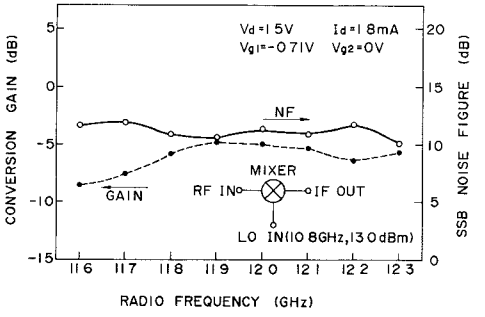


Fig. 9. Frequency characteristics for mixer without buffer.

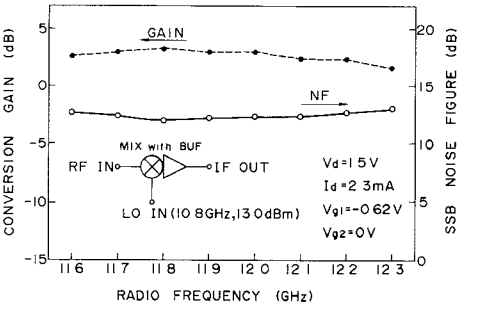


Fig. 10. Frequency characteristics for mixer with buffer.

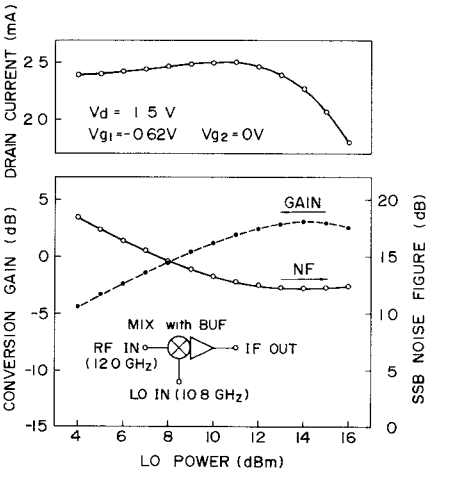


Fig. 11. LO power characteristics for mixer with buffer.

Fig. 8 shows a key process for the closely spaced electrode FET. Al is deposited by evaporation on the ion-implanted GaAs wafer. To form gates, the Al is etched, using a photo-resist mask to give the ohmic contact pattern. Ohmic contact is made by evaporating AuGe-Ni. The evaporation is carried out with the same photo-resist mask used in the Al etching. By controlling the side etching of Al, gate and ohmic spacings can be shortened to 0.5 μm in a self-aligned manner. The evaporated AuGe-Ni is lifted-off and then alloyed. The Al is etched selectively again to remove unnecessary parts.

IV. Microwave Performance

A. Mixer

The IC chips were chosen for microwave evaluation on the basis of visual inspection and dc testing. The selected chips were mounted on Au-plated copper carriers using an AuSn solder. The carriers were then mounted on test fixtures and tested in a 50-Ω system.

Fig. 9 shows gain and noise figure versus frequency characteristics for the mixer chip alone. It provides a 6.1 ± 1.5-dB conversion loss with an 11.1 ± 0.6-dB SSB noise figure in the 11.7 to 12.2-GHz RF band, which is the designed frequency band. Bias conditions are shown in the figure. The optimal noise figure was obtained when the first gate bias voltage was near pinchoff, and is the same as the reported result [1]. For the second gate, performances were scarcely varied in the vicinity of 0-V bias voltage. Therefore, measurements were carried out while grounding the second gate.

LO power was set at 13 dBm, where the optimal performance was obtained. When 13-dBm LO power was supplied, leaked LO power was -5.3 dBm at the RF port and -11.7 dBm at the IF port.

Fig. 10 shows frequency characteristics when connecting the buffer chip. The mixer and buffer chips were mounted adjacently on the carrier and connected by Au bonding wire. It provides 2.9 ± 0.4-dB conversion gain with 12.3 ± 0.3-dB SSB noise figure in the same frequency band.

Fig. 11 shows gain, noise figure, and drain current versus LO power characteristics for the mixer with the buffer. Bias conditions were set at the same values as for the Fig. 10 case. RF is 12.0 GHz. Optimal performance is obtained when the LO power is 13 to 15 dBm.

Fig. 12 shows RF input power and drain current versus IF output power characteristics. The IF output power at 1-dB gain compression is -1.2 dBm. This value is determined by the mixer chip, and is about 5 dB lower than that for the same gate width FET amplifier case. One reason for the lower saturation power could be due to the near pinchoff biasing for the first gate.

Fig. 13 shows input impedance for the mixer RF port. The reference plane is chosen at the cleaved edge of the mixer chip. In the 11.7–12.2-GHz band, less than 1.5 VSWR is obtained. For the LO port, however, input VSWR is about 6 at the LO frequency of 10.8 GHz. Therefore, a half of the LO power is reflected at the LO input port.

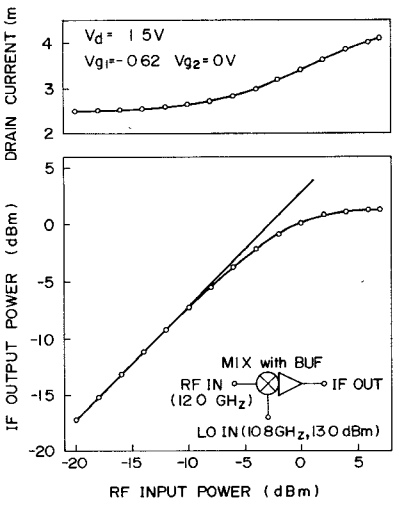


Fig. 12. RF power characteristics for mixer with buffer.

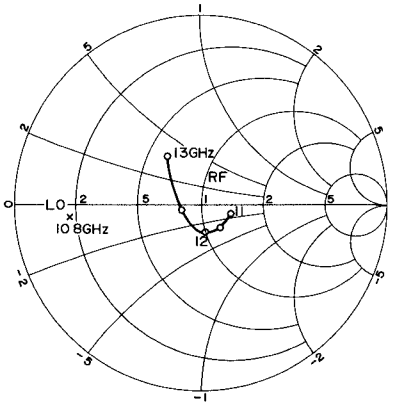


Fig. 13. Mixer RF port input impedance.

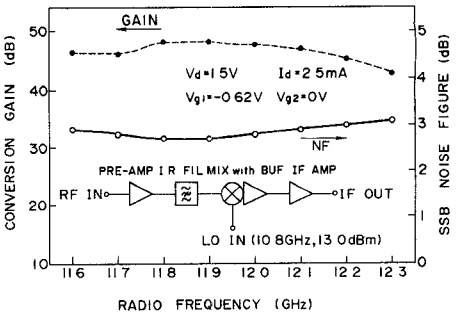


Fig. 14. Frequency characteristics for low-noise converter.

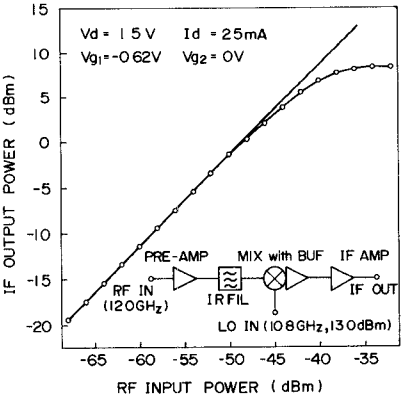


Fig. 15. RF power characteristics for low-noise converter.

B. Low-Noise Converter

A low-noise converter was constructed by using the mixer to examine the performances. A block-diagram for the converter is shown in Fig. 14. All components, except the image-rejection filter, are realized by GaAs monolithic IC's. The IC fabrication processes are identical to the process used for the mixer. The preamplifier is constructed by cascade connection of one- and two-stage amplifiers. The one-stage amplifier has more than 9.5-dB gain with less than 2.5-dB noise figure. The two-stage amplifier has more than 16-dB gain with less than 2.8-dB noise figure in the 11.7–12.7-GHz band [4]. As the image-rejection filter, a commercially available bandpass filter was used. The filter provides more than 69-dB image rejection. The IF amplifier is a resistor–capacitor coupled-type two-stage amplifier and it has 16-dB gain with 3-dB noise figure in the 9 MHz–3.9-GHz band [5].

Fig. 14 shows gain and SSB noise-figure versus frequency characteristics for the converter. It provides 46.8 ± 1.5-dB conversion gain with 2.8 ± 0.2-dB SSB noise figure in the 11.7–12.2-GHz desired frequency band. Bias conditions for the mixer are shown in the figure.

Fig. 15 shows RF input power versus IF output power characteristics. The IF output power at 1-dB gain compression is 4.7 dBm, and about 8 dBm at saturation. These values are determined by the IF amplifier. Therefore, the values can be improved by increasing saturation power for the IF amplifier.

V. Conclusion

The design considerations, fabrication process, and microwave performances for newly developed 12-GHz-band GaAs dual-gate MESFET monolithic mixers for use in DBS receivers have been described. Small chip size was achieved by connecting a buffer amplifier with high input impedance directly after the mixer IF port and removing the IF matching circuit. For the interstage circuit between the mixer and the IF amplifier, effects on mixer performances were investigated. The results indicate that matching to 50 Ω does not improve performances, as long as a resistor–capacitor coupled-type IF amplifier is employed.

The mixer was fabricated by means of a well-established IC process, using an ion-implanted closely spaced electrodes FET. The mixer provides 2.9 ± 0.4-dB conversion gain with 12.3 ± 0.3-dB SSB noise figure. A low-noise converter was constructed by connecting a monolithic preamplifier, an image-rejection filter, and a monolithic IF amplifier to the mixer. The converter provides 46.8 ± 1.5-dB conversion gain with 2.8 ± 0.2-dB SSB noise figure. These performances are well within the acceptable range for DBS receivers. This work has made a cost-effective one-chip front-end for DBS systems more realistic.

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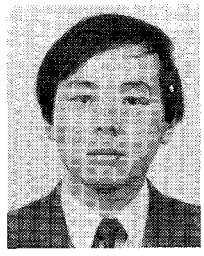

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